ACADEMIC REGULATIONS (R-20)
COURSE STRUCTURE
AND
DETAILED SYLLABI

M.Tech Regular (Full Time) Two Year Post Graduate Degree Programme

(For the Batches Admitted From the Academic Year 2020-2021)

VLSI DESIGN

Department of Electronics and Communication Engineering

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

Accredited by NBA, New Delhi, Accredited by NAAC, Bengaluru |Affiliated to JNTUA, Ananthapuramu, Recognized by UGC under 12(B) & 2(F) | Approved by AICTE, New Delhi

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FOREWORD

The autonomy is conferred on Sri Venkateswara College of Engineering and technology by JNT University, Anantapur based on its performance as well as future commitment and competency to impart quality education. It is a mark of its ability to function independently in accordance with the set norms of the monitoring bodies like UGC and AICTE. It reflects the confidence of the affiliating University in the autonomous institution to uphold and maintain standards it expects to deliver on its own behalf and thus awards degrees on behalf of the college. Thus, an autonomous institution is given the freedom to have its own curriculum, examination system and monitoring mechanism, independent of the affiliating University but under its observance.

Sri Venkateswara College of Engineering and Technology is proud to win the confidence of all the above bodies monitoring the quality in education and has gladly accepted the responsibility of sustaining, the standards and ethics for which it has been striving for more than a decade in reaching its present standing in the arena of contemporary technical education. As a follow up, statutory bodies like Academic Council and Boards of Studies are constituted with the guidance of the Governing Body of the College and recommendations of the JNTUA, Anantapur to frame the regulations, course structure and syllabi under autonomous status.

The autonomous regulations, course structure and syllabi have been prepared after prolonged and detailed interaction with several expertise solicited from academics, industry and research, to produce quality engineering graduates to the society.

All the faculty, parents and students are requested to go through all the rules and regulations carefully. Any clarifications needed are to be sought at appropriate time and with principal of the college, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The cooperation of all the stake holders is sought for the successful implementation of the autonomous system in the larger interests of the college and brighter prospects of engineering graduates.

VISION AND MISSION OF THE INSTITUTE UNDER R20 REGULATIONS

INSTITUTION VISION:

- Carving the youth as dynamic, competent, valued and knowledgeable professionals who shall lead the Nation to a better future and to mould the institute into a Center of Academic Excellence and advanced Research

INSTITUTION MISSION:

- Providing Quality Education, student-centered teaching-learning processes and state of-art infrastructure for professional aspirants hailing from both rural and urban areas.
- Imparting technical education that encourages independent thinking, develops strong domain of knowledge, hones contemporary skills and positive attitudes towards holistic growth of young minds.

QUALITY POLICY

Sri Venkateswara College of Engineering and Technology strides towards excellence by adopting a system of qualitative policies and processes with continued improvements to enhance students' skills and talents for their exemplary contribution to the society, the nation and the world.

SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY
(AUTONOMOUS)
(AFFILIATED TO JNTUA, ANANTAPUR)
ACADEMIC REGULATIONS – R20
MASTER OF TECHNOLOGY (M.TECH)
REGULAR (Full-Time) TWO YEAR POST GRADUATE DEGREE PROGRAMME
(For the batches admitted from the Academic Year 2020-2021)

The Jawaharlal Nehru Technological University Anantapur, Ananthapuramu shall confer M.Tech Post Graduate degree to candidates who are admitted to the Master of Technology Program and fulfill all the requirements for the award of the degree.

1.0 **Applicability:** All the rules specified herein, approved by the Academic Council, shall be in the force and applicable to the students admitted from the Academic Year 2020-2021 onwards. Any reference to "College" in these rules and regulations stands for SVCET.

2.0 **Extent:** All the rules and regulations, specified hereinafter shall be read as a whole for the purpose of interpretation. As and when a doubt arises, the interpretation of the Chairman, Academic Council shall be final and ratified by the Academic Council in the forthcoming meeting. As per the requirements of statutory bodies, Principal, Sri Venkateswara College of Engineering College shall be the Chairman, Academic Council.

3.0 **Admission:** Admission into the first year of two year M.Tech degree programme is based on the eligibility conditions detailed below.

4.0 **Eligibility:**
Admission to the above programme shall be made subject to the eligibility, qualifications and specialization prescribed by the competent authority for each programme, from time to time. Admissions shall be made either on the basis of merit rank obtained by the qualified candidates at an Entrance Test conducted by the University or on the basis of GATE / PGECET score, subject to reservations and policies prescribed by the Government from time to time.

4.1 **Admission Procedure:**
As per the existing stipulations of AP State Council for Higher Education (APSCHE), Government of Andhra Pradesh, admissions are made into the first year as follows:
a) Category –A seats are to be filled by Convenor through APPGECET / GATE score.
b) Category-B seats are to be filled by Management as per the norms stipulated by Government of A.P.

5.0 **Specializations:**

S. No.	Branch	Specialization
1	CE	Structural Engineering
2	EEE	PE&ED
3	ME	CAD/CAM
4	ECE	VLSI Design
5	CSE	Computer Science and Engineering
6	CSE	CSE(Data Science)

6.0 **Course Work:**
A Candidate after securing admission must pursue the M.Tech course of study for Four Semesters duration. Each semester shall have a minimum of 16 instructional weeks.
A candidate admitted to a programme should complete it within a period equal to twice the prescribed duration of the programme from the date of admission.

7.0 **Contact Periods:**
Depending on the complexity and volume of the course, the numbers of contact periods per week are assigned.

7.1 **Credit Courses:** Courses are to be registered by a student in a Semester to earn Credits. Credits shall be assigned to each Course in an L: T: P: C (Lecture Hours: Tutorial Hours: Practical Hours: Credits) structure, based on the following pattern.

7.2 **Theory Courses:** One hour Lecture (L) per Week in a Semester = 01 Credit.

7.3 **Practical Courses:** One Practical hour (P) per Week in a Semester = 0.5 Credit.

7.4 **Audit Courses (AC) = NOCREDITS** are awarded

7.5 **Mini Project:** For Mini Project, where formal contact periods are not specified, credits are assigned based on the complexity of the work to be carried out.

7.6 **Dissertation Work:** For Dissertation Work, where formal contact periods are not specified, credits are assigned based on the complexity of the work to be carried out.

7.7 The Two year curriculum of Post Graduate Degree Program M. Tech shall have total of 68 credits.

8.0 Choice Based Credit System (CBCS):

8.1 Choice Based Credit System (CBCS) is introduced in line with UGC guidelines in order to promote:

- Student centered learning
- Students to learn courses of their choice

A Student has a choice of registering for courses comprising basic science, program core and professional elective.

9.0 Evaluation:

The performance of the candidate in each semester shall be evaluated subject wise, with a maximum of 100 marks for Theory and 100 marks for practical's, on the basis of Internal Evaluation and End Semester Examination.

For the theory subjects, 60% of the marks will be for the External End Examination. While 40% of the marks will be for Internal Evaluation. Internal marks for midterm examinations shall be arrived at by considering the marks secured by the student in both the midterm examinations with 80% weightage to the better midterm exam and 20% to the other. First midterm examinations will be conducted in the middle of the Semester (first two units) and second midterm examinations immediately after the completion of instruction (last three units) with four questions with internal choice, either or type, are to be answered in 2 hours, evaluated for 40 marks.

For semester end examination five questions shall be given for a maximum of 60 marks with one question from each unit with internal choice i.e. either or type. All questions carry equal marks.

For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks will be for internal evaluation based on the day to day performance (25 marks) and practical test at the end of the semester (15 marks).

For Mini Project there will be an internal evaluation for 100 marks. A candidate has to secure a minimum of 50% to be declared successful. The assessment will be made by a board consisting of HOD, Mini Project supervisor and one senior faculty of the department.

A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

In case the candidate does not secure the minimum academic requirement in any of the subjects, he has to reappear for the Semester Examination either supplementary or regular in that subject, or repeat the subject when next offered or do any other specified subject as may be required.

In case of audit course, students will be able to register for courses outside the prescribed range of Credits for audit only, when interested to supplement their knowledge / skills; any student who wishes to pursue audit course can register for the same with the concerned teacher and attend to the classes regularly. No examination will be conducted; no grade will be given for the audit courses. However such of those students who have registered and got the requisite attendance of 75% in the audit course, it will be mentioned in their grade sheet.

10.0 Dissertation Work:

10.1 Registration of Dissertation work

A candidate shall register for the dissertation work at the beginning of the second year, only after satisfying the attendance requirement of all the courses up to II Semester. The duration of the dissertation work is for two semesters.

10.2 The candidate has to submit, in consultation with the supervisor, the title, objective and plan of action of dissertation work to the Department Evaluation Committee (DEC) for its approval. Only after obtaining the approval from DEC, the student can initiate the dissertation work.

11.0 Evaluation of Dissertation Work

11.1 The Department Evaluation Committee (DEC) consisting of HOD, Supervisor and one internal senior

faculty member shall monitor the progress of the project work. The DEC is constituted by the Principal on the recommendation of the Head of the Department.

11.2 Dissertation work Phase – I is to be completed in the III Semester. The student has to identify the topic of the project work, collect relevant literature, preliminary data, implementation tools/methodologies etc., and perform a critical study and analysis of the problem identify and submit a report.

(i) Internal Evaluation: The internal evaluation of dissertation work phase – I shall be made by the DEC on the basis of two project reviews on the topic of the project. Each review shall be conducted for a maximum of 40 marks. For a total of 40 marks, 80% of better one of the two and 20% of the other one are added and finalized.

(ii) Semester-End Evaluation: The Semester end dissertation work phase – I Viva-Voce examination shall be conducted for 60 marks, by the HOD, concerned supervisor and a senior faculty member recommended by the HOD and appointed by the Principal.

11.**3** The student shall continue to undertake the dissertation work phase – II during the IV Semester by conducting practical investigations, implementation, analysis of results, validation and report writing. The student shall submit a dissertation report at the end of the semester after approval of the DEC.

(i) Internal Evaluation: The internal evaluation of dissertation work phase – II shall be made by the DEC on the basis of two project reviews on the progress, presentation and quality of work. Each review shall be conducted for a maximum of 120 marks. For a total of 120 marks, 80% of better one of the two and 20% of the other one are added and finalized.

(ii) Semester-End Evaluation: A candidate shall be allowed to submit the dissertation on the recommendations of the DEC. Three copies of the Dissertation certified in the prescribed format by the concerned Supervisor and HOD shall be submitted to the department. The Department shall submit a panel of three experts for a maximum of 05 students to the principal for appointment of the external examiner. The Viva-voce examination shall be conducted by the board consisting of the Supervisor, Head of the Department and the external examiner nominated by the principal. The board shall jointly award the marks for 180.

11.4 A candidate shall be deemed to have secured the minimum academic requirement of project work if he secures a minimum of 40% marks in the viva-voce examination and a minimum aggregate of 50% of the total marks in the end viva-voce examination and the internal assessment marks taken together. If he fails to get the minimum academic requirement he has to appear for the viva-voce examination again to get the minimum marks. The viva voce examination may be conducted once in two months for all the candidates who have submitted thesis during that period.

12.0 Eligibility to appear for the Semester-End Examination (SEE)

12.1 A student shall be eligible to appear for semester-end examinations if he acquires a minimum of 75% of attendance in aggregate of all the courses in a semester.

12.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below75%) in each semester may be granted by the College Academic Council.

12.3 Shortage of Attendance below 65% in aggregate shall **in no case be condoned**.

12.4 Student whose shortage of attendance is not condoned in any semester is not eligible to take their end examination of that class and their registration shall stand cancelled.

12.5 A student shall not be promoted to the next semester unless he satisfies the attendance requirements of the current semester, as applicable. The student may seek readmission for the semester when offered next. He will not be allowed to register for the courses of the semester while he is in detention. A student detained due to shortage of attendance, will have to repeat that semester when offered next.

12.6 A stipulated fee shall be payable to the College towards condonation of shortage of attendance.

12.7 The attendance in Student Development Activities shall be considered for finalization of aggregate attendance.

12.8 For the calculation of a student attendance in any semester, the total number of classes conducted shall be counted as scheduled in the class-work time table.

13.0 Conduct of Semester End Examination and Evaluation

13.1 Semester end examination shall be conducted by the Controller of Examination (COE) by inviting 50% Question Papers from the External and 50% Question papers from the Internal Subject Experts. Principal will decide the External and Internal subject experts.

13.2 The answer papers of semester end examination should be evaluated externally / internally.

13.3 Marks for components evaluated internally by the faculty shall be submitted to the Controller of Examinations one week before the commencement of the End examinations. The marks for the internal evaluation components shall be added to the external evaluation marks secured in the Semester-end examinations, to arrive at the total marks for any course in that semester.

13.4 Performance in all the subjects is tabulated program-wise and will be scrutinized by the office of the Controller of Examinations. Total marks obtained in each subject are converted into letter grades. Finally subject-wise marks and grades details, subject-wise and branch-wise pass percentages are calculated through software.

14.0 Results Committee

14.1 Results Committee comprising of Principal, Controller of Examinations, Additional Controller of Examinations (Confidential) and one Senior Professor nominated by the Principal and the University Nominee will oversee the details of marks, grades and pass percentages of all the subjects and branch-wise pass percentages.

14.2 Office of the Controller of Examinations will generate student-wise result sheets and the same will be published through college website.

14.3 Student-wise Grade Sheets are generated and issued to the students.

15.0 Personal Verification / Recounting / Revaluation / Final Valuation

15.1 **Personal Verification of Answer Scripts:**

Candidates appear in a particular semester end examinations may appeal for verification of their answer script(s) for arithmetic correction in totaling of marks and any omission / deletion in evaluation within 7 days from the date of declaration of results at the office of the Controller of Examinations on the prescribed proforma and by paying the prescribed fee per answer script.

It is clarified that personal verification of answer script shall not tantamount to revaluation of answer script. This is only a process of reverification by the candidate. Any mistake / deficiency with regard to arithmetic correction in totaling of marks and any omission / deletion in evaluation if found, the institution will correct the same.

15.2 **Recounting / Revaluation:**

Students shall be permitted for request for recounting/revaluation of the Semester-End examination answer scripts within a stipulated period after payment of prescribed fee. After recounting or revaluation, records are updated with changes if any and the student will be issued a revised grade sheet. If there are no changes, the same will be intimated to the students.

15.3 **Final Valuation:**

Students shall be permitted for request for final valuation of the Semester–End Examination answer scripts within a stipulated period after the publication of the revaluation results by paying the necessary fee. The final valuation shall be carried out by an expert not less than Associate Professor as per the scheme of valuation supplied by the examination branch in the presence of the student, Controller of Examinations and Principal. However students are not permitted to discuss / argue with the examiner. If the increase in marks after final valuation is equal to or more than 15% of the previous valuation marks, the marks obtained after final valuation shall be treated as final. If the variation of marks after final valuation is less than 15% of the previous valuation marks, then the earlier valuation marks shall be treated as the final marks.

16.0 Supplementary Examinations: In addition to the regular semester-end examinations conducted, the College may also schedule and conduct supplementary examinations for all the courses of other semesters when feasible for the benefit of students. Such of the candidates writing supplementary examinations may have to write more than one examination per day.

17.0 Re-Registration for improvement of Internal Marks

17.1 Following are the conditions for Re-Registration of Theory Courses for improvement of Internal Marks:

17.2 The student should have completed all the course work and obtained examinations results from I to III semesters.

17.3 If the student has failed in the examination due to internal evaluation marks secured being less than

50%, he shall be given one chance for a maximum of 3 theory courses for improvement of internal evaluation marks.

17.4 The candidate has to register for the chosen courses and fulfill the academic requirements (i.e. a student has to attend the classes regularly and appear for the mid-examinations and satisfy the attendance requirements to become eligible for appearing at the semester-end examinations).

17.5 For each course, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D./ Challan in favour of the Principal, Sri Venkateswara College of Engineering & Technology, payable at Chittoor along with the requisition through the concerned Head of the Department.

17.6 A student availing the benefit for Improvement of Internal evaluation marks, the internal evaluation marks as well as the semester-end examinations marks secured in the previous attempt(s) for the re-registered courses stands cancelled.

18.0 Academic Requirements for completion of Post Graduate Degree Program M.Tech:

The following academic requirements have to be satisfied in addition to the attendance requirements for completion of Post Graduate Degree Program M.Tech.

For students admitted into Post Graduate Degree Program M.Tech for the Academic Year 2020-21:

18.1 A student shall be deemed to have satisfied the minimum academic requirements for each theory, laboratory course, and Internship and project work, if he secures not less than 40% of marks in the semester-end examination and a minimum of 50% of marks in the sum total of the internal evaluation and Semester-end examination taken together.

A student shall be deemed to have satisfied the minimum academic requirements of mini-project, if he secures not less than a minimum of 50% of marks.

18.2 A student shall register for all the **68** credits and earn all the **68** credits. Grade points obtained in all the 6**8** credits shall be considered for the calculation of the DIVISION based on CGPA.

18.3 A student who fails to earn **68** credits as indicated in the course structure within **four** academic years from the year of their admission shall forfeit his seat in M.Tech Program and his admission stands cancelled.

19.0 Grades, Semester Grade point Average, Cumulative Grade point Average:

19.1 **Grade System:** After all the components and sub-components of any subject (including laboratory subjects) are evaluated, the final total marks obtained will be converted to letter grades on a "10 point scale" described below.

% of Marks obtained	Grade	Grade Points (GP)
90 to 100	A+	10
80 to 89	A	9
70 to 79	B	8
60 to 69	C	7
50 to 59	D	6
Less than 50%in Sum of Internal & External (or) Less than 40% in External	F	0
Not Appeared	N	0

19.2 Computation of SGPA and CGPA

19.2.1 The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.

$$\mathbf{SGPA = \Sigma (Ci \times Gi) / \Sigma Ci}$$

where, Ci is the number of credits of the i^{th} subject and Gi is the grade point scored by the student in the i^{th} course

19.2.2 The Cumulative Grade Point Average (CGPA) will be computed in the same manner taking into account all the courses undergone by a student over all the semesters of a program, i.e.

$$\mathbf{CGPA = \Sigma (Ci \times Si) / \Sigma Ci}$$

where ‘Si’ is the SGPA of the ith semester and Ci is the total number of credits in that semester

19.2.3 Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.

19.2.4 While computing the SGPA/CGPA, the subjects in which the student is awarded Zero grade points will also be included.

19.2.5 Grade Point: It is a numerical weight allotted to each letter grade on a 10-point scale.

19.2.6 **Letter Grade:** It is an index of the performance of students in a said course. Grades are denoted by letters A+, A, B, C, D, F and N.

19.2.7 As per AICTE regulations, conversion of CGPA into equivalent percentage is as follows:

Equivalent Percentage to SGPA = (SGPA – 0.50) x 10
Equivalent Percentage to CGPA = (CGPA – 0.50) x 10

19.3 **Grade Sheet:** A grade sheet (Marks Memorandum) will be issued to each student Indicating his performance in all subjects registered in that semester indicating the GPA and CGPA. GPA and CGPA will be rounded off to the second place of decimal.

20.0 **Consolidated Grade Sheet:** After successful completion of the entire Program of study, a Consolidated Grade Sheet containing performance of all semesters will be issued as a final record. Duplicate Consolidated Grade Sheet will also be issued, if required, after payment of requisite fee.

21.0 **Award of Degree:** The Degree will be conferred and awarded by Jawaharlal Nehru Technological University Anantapur, Ananthapuramu on the recommendation of The Principal of SVCET (Autonomous). Student admitted in M.Tech 2Yrs programme shall register for all **68** credits and earn all the **68** credits. Marks obtained in all the **68** credits shall be considered for the award of the class based on CGPA.

21.1 **Eligibility:** A student shall be eligible for the award of M.Tech Degree if he fulfills all the following conditions:

- Registered and successfully completed all the components prescribed in the program of study for which he is admitted.
- Successfully acquired the minimum required credits as specified in the curriculum corresponding to the branch of study within the stipulated time.
- Obtained CGPA greater than or equal to 6.0 (Minimum requirement for declaring as passed.)

21.2 **Award of Class:** Declaration of Class is based on CGPA.

Cumulative Grade Point Average	Class
≥7.75	First Class with Distinction
≥6.75 and<7.75	First Class
≥6.0 and <6.75	Second Class

22.0 **With Holding of Results:**
If the candidate has not paid dues to the University / College or if any case of in-discipline is pending against him, the result of the candidate shall be withheld and he will not be allowed / promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

23.0 **Graduation Day:**
The institute shall have its own annual Graduation Day for the award of Provisional Certificates to students completing the prescribed academic requirements in each case, in consultation with the University and by following the provisions in the Statute. The college shall institute prizes and medals to meritorious students and award them annually at the Graduation Day. This will greatly encourage the students to strive for excellence in their academic work.

24.0 **Discipline:**
Every student is required to observe discipline and decorum both inside and outside the institute and not to indulge in any activity which will tend to bring down the honor of the institute. If a student indulges

in malpractice in any of the theory / practical examination, continuous assessment examinations he shall be liable for punitive action as prescribed by the Institute from time to time.

25.0 Grievance Redressal Committee:

The institute shall form a Grievance Redressal Committee for each course in each department with the Course Teacher and the HOD as the members. This Committee shall solve all grievances related to the course under consideration.

26.0 Transitory Regulations:

Students who got detained for want of attendance (**or**) who have not fulfilled academic requirements (**or**) who have failed after having undergone the Program in earlier regulations (**or**) who have discontinued and wish to continue the Program are eligible for admission into the unfinished semester from the date of commencement of class work with the same (**or**) equivalent courses as and when courses are offered and they will be in the academic regulations into which they are presently readmitted. A student has to satisfy all the eligibility requirements within the maximum stipulated period of **four years** for the award of M.C.A Degree.

27.0 Medium of Instruction:

The Medium of Instruction is **English** for all courses, laboratories, Internal and External examinations, Seminar Presentation and Project Reports.

28.0 Mode of Learning:

Preferably 50% course work for the theory courses in every semester shall be conducted in the blended mode of learning. If the blended learning is carried out in online mode, then the total attendance of the student shall be calculated considering the offline and online attendance of the student.

29.0 General Instructions:

i. The academic regulations should be read as a whole for purpose of any interpretation.

ii. Disciplinary action for Malpractice/improper conduct in examinations is appended.

iii. Where the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

iv. In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

v. The Principal may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the Principal.

vi. The above rules and regulations are to be approved / ratified by the College Academic Council as and when any modification is to be done.

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FAILURE TO READ AND UNDERSTAND THE REGULATIONS IS NOT AN EXCUSE

SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY
(AUTONOMOUS)
(AFFILIATED TO JNTUA, ANANTHAPURAMU)

RULES FOR DISCIPLINARY ACTION FOR MALPRACTICE / IMPROPER CONDUCT IN EXAMINATIONS

Sl.No.	Nature of Malpractices / Improper conduct If the candidate	Punishment
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination).	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester / year. The Hall Ticket of the candidate is to be cancelled.
3.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester / year.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that Semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that Semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
6.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that Semester/year.

		The candidate is also debarred and forfeits of seat.
7.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the impostor is an outsider, he will be handed over to the police and a case is registered against him.
8.	Refuses to obey the orders of the Chief Superintendent / Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in-charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction or property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate (s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester / year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester / year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the Examination committee for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.

SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY
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Identification of Courses

M. Tech

Each course shall be uniquely identified by an alphanumeric code of width 7 characters as given below.

No. of Digits	**Description**
First two digits	Year of regulations Ex:20
Next one letter	Type of program: A: B. Tech B: M. Tech C: M.B.A D: M.C.A
Next two letters	Code of program: ST: Structural Engineering, P.E: Power Electronics & Electric Drives, CM: CAD/CAM, VL: VLSI, CS: Computer Science and Engineering, DS: Data Science
Last two digits	Indicate serial numbers: ≥ 01

Ex:
20BST01
20BPE01
20BCM01
20BVL01
20BCS01
20BDS01

Department Vision & Mission under R-20 Regulations

VISION

To become a centre of excellence in the field of electronics and communications offering higher order of learning and conducting contemporary research thereby producing globally competitive and ethically strong engineering professionals.

MISSION

- Establish a scintillating learning environment to produce quality graduates with passion for knowledge and creativity in the field of Electronics and Communication Engineering.
- Impart quality education through periodically updated curriculum to meet the challenges of the industry and research at the global level.
- Enhancing employability of the students by providing skills through comprehensive experiential learning.
- Developing professional etiquette and ethical integrity among the students to face real-time life challenges.
- Empower the faculty through continuous training in domain, research and pedagogy for enhancing learning outcomes of the students and Research output.

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(AUTONOMOUS)

Program Education Objectives (PEOs)

PEO – 1

Identify and apply appropriate Electronic Design Automation (EDA) to solve real world problems in VLSI domain to create innovative products and systems.

PEO – 2

Develop managerial skill and apply appropriate approaches in the domains of VLSI design incorporating safety, sustainability and become a successful professional or an Entrepreneur in the domain.

PEO – 3

Pursue career in research in VLSI Design domain through self learning and self directed on cutting edge technologies.

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(AUTONOMOUS)

Program Outcomes of M.Tech-VLSI Design

1. Independently carry out research /investigation and development work to solve practical problems related to VLSI Design.

2. Write and present a substantial technical report/document in the field of VLSI Design.

3. Demonstrate a degree of mastery over the areas of VLSI Design. The mastery should be at a level higher than the requirements in the bachelor's in Electronics & Communication Engineering.

4. Propose and execute optimal solutions for problems in the field of VLSI design.

5. Apply appropriate methodology and modern engineering/IT tools to meet the international standards in the area of VLSI design.

6. Acquire integrity and ethics of research to execute projects efficiently.

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Program Specific Outcomes of M.Tech-VLSI Design

1. Acquire competency in areas of VLSI, IC Fabrication, Design, Testing, Verification and prototype development focusing on applications.

2. An exposure to variety of programming languages and software's.

SRI VENKATESWARA COLLEGE OF ENGINEERING & TECHNOLOGY

(AUTONOMOUS)
R.V.S. NAGAR, CHITTOOR - 517127, A.P.

COURSE STRUCTURE AND SCHEME OF EXAMINATION FOR M.TECH-VLSI DESIGN UNDER ACADEMIC REGULATIONS R20

M.TECH, I-SEMESTER

S.NO	SUBJECT CODE	SUBJECT	PERIODS			CREDITS	SCHEME OF EXAMINATION (MAXIMUM MARKS)		
			L	T	P		CIE	SEE	TOTAL
1	20BVL01	VLSI Technology	3	0	0	3	40	60	100
2	20BVL02	Analog IC Design	3	0	0	3	40	60	100
PROFESSIONAL ELECTIVE – I									
3	20BVL03	Digital IC Design	3	0	0	3	40	60	100
	20BVL04	VLSI for wireless communication							
	20BVL05	Hardware Software Co-Design							
PROFESSIONAL ELECTIVE – II									
4	20BVL06	Embedded System Design	3	0	0	3	40	60	100
	20BVL07	Hardware Description Languages							
	20BVL08	Image Processing and Pattern Recognition							
5	20BMB21	Research Methodology	2	0	0	2	40	60	100
6	20BVL09	Digital System Design Lab	0	0	4	2	40	60	100
7	20BVL10	VLSI system design lab	0	0	4	2	40	60	100
8	20BVL11	Audit Course: Human values and professional ethics	2	0	0	-	-	-	-
TOTAL			**16**	**0**	**8**	**18**	**280**	**420**	**700**

M.TECH, II-SEMESTER

S.NO	SUBJECT CODE	SUBJECT	PERIODS			CREDITS	SCHEME OF EXAMINATION (MAXIMUM MARKS)		
			L	T	P		CIE	SEE	TOTAL
1	20BVL12	Low Power VLSI Design	3	0	0	3	40	60	100
2	20BVL13	Algorithms for VLSI Design Automation	3	0	0	3	40	60	100
PROFESSIONAL ELECTIVE – III									
3	20BVL14	Nano Electronics	3	0	0	3	40	60	100
	20BCS13	Cryptography and Network Security							
	20BVL15	Scripting Language for VLSI Design Automation							
PROFESSIONAL ELECTIVE – IV									
4	20BVL16	DSP Processors & Architectures	3	0	0	3	40	60	100
	20BVL17	Design of semiconductor memories							
	20BVL18	Electronic Design Automation Tools							
5	20BVL19	Mini Project	0	0	4	2	100	00	100
6	20BVL20	Mixed Signal Lab	0	0	4	2	40	60	100
7	20BVL21	Embedded Systems Lab	0	0	4	2	40	60	100
8	20BVL22	Audit Course: Intellectual property rights	2	0	0	-	-	-	-
TOTAL			**14**	**0**	**12**	**18**	**340**	**360**	**700**

M.TECH, III SEMESTER

S.NO	SUBJECT CODE	SUBJECT	PERIODS			CREDITS	SCHEME OF EXAMINATION (MAXIMUM MARKS)		
			L	T	P		CIE	SEE	TOTAL
PROFESSIONAL ELECTIVE – V									
1	20BVL23	FPGA Architectures & Applications	3	0	0	3	40	60	100
	20BVL24	Testing & Testability							
	20BVL25	ASIC Design							
PROFESSIONAL ELECTIVE – VI									
2	20BVL26	High Speed Networks	3	0	0	3	40	60	100
	20BVL27	System on chip design and verification							
	20BVL28	RF IC Design							
3	20BVL29	**DISSERTATION PHASE-I**	-	-	20	10	40	60	100
TOTAL			**6**	**0**	**20**	**16**	**120**	**180**	**300**

M.TECH, IV-SEMESTER

S.NO	SUBJECT CODE	SUBJECT	PERIODS			CREDITS	SCHEME OF EXAMINATION (MAXIMUM MARKS)		
			L	T	P		CIE	SEE	TOTAL
1	20BVL30	**DISSERTATION PHASE-II**	-	-	32	16	120	180	300
TOTAL						**16**	**120**	**180**	**300**

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M.Tech- I Semester-VLSI Design	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

Outcomes:

On successful completion of the course the student will be able to

1. Gain knowledge of different VLSI fabrication processes and CMOS Logic Design.
2. Design different MOS logical circuits.
3. Gain knowledge on the various tools in the layout analysis
4. Gain knowledge about Floor planning methods.

(20BVL01) VLSI TECHNOLOGY

UNIT I

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: Technology (MOS, CMOS, Bi-CMOS) Trends and Projections.

BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS: Ids-Vds Relationships, Threshold Voltage V_t, G_m, G_{ds} and W_o, Pass Transistor, MOS,CMOS & Bi-CMOS Inverters, Z_{pu}/Z_{pd}, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT II

LAYOUT DESIGN AND TOOLS: Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT III

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

UNIT IV

SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT V

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SoCs and Embedded CPUs,

Architecture Testing.

TEXT BOOKS:

1. K. Eshraghian et . al, "Essentials of VLSI Circuits and Systems" , PHI of India Ltd.,2005.
2. Wayne Wolf, "Modern VLSI Design", 4th Edition, Prentice Hall Modern Semiconductor Design , 2008.

REFERENCES:

1. N.H.E Weste, K.Eshraghian, "Principals of CMOS Design", Adison Wesley, 2ndEdition.
2. Fabricius, "Introduction to VLSI Design", MGH International Edition, 1990.
3. Baker, Li Boyce, "CMOS Circuit Design, Layout and Simulation", PHI, 2004.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	1	2	2	2	2	3	2
CO2	2	1	2	2	2	2	2	2
CO3	2		3	3	2	2	2	2
CO4	2	1	2	2	2	2	2	2

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M.Tech- I Semester-VLSI Design

L	T	P	C
3	0	0	3

(20BVL02) ANALOG IC DESIGN

Outcomes:

On successful completion of the course the student will be able to

1. Gain knowledge of different Interpolating, Folding and Pipelining techniques.
2. Design different Sample and Hold Switched Capacitor Circuits.
3. Analyze the various CMOS various operational amplifiers
4. Understand about operation of data converters.

UNIT I

MOS TRANSISTORS, MODELLING AND CURRENT MIRROR:

MOS Transistors- Modeling in Linear and Saturation Regions, Advanced MOS Modeling, Simple CMOS Current Mirror, Common-Source Amplifier, Source-Follower or Common-Drain Amplifier, Common-Gate Amplifier, Source-Degenerated Current Mirrors, Cascade Current Mirrors and Cascade Gain Stage.

UNIT II

OPERATIONAL AMPLIFIER DESIGN, COMPENSATION AND COMPARATORS: Two-Stage CMOS Opamp, Opamp Compensation, Advanced Current Mirrors, Folded-Cascade Opamp, Current Mirror Opamp, Fully Differential Opamps, Common-Mode Feedback Circuits. Comparator Specifications, Charge-Injection Errors, Latched Comparators and Examples of CMOS and Bi-CMOS Comparators.

UNIT III

SAMPLE AND HOLDS AND SWITCHED CAPACITOR CIRCUITS: Performance of Sample-and-Hold Circuits, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Bipolar and Bi-CMOS Sample and Holds.

Switched Capacitor Circuits: Basic Building Blocks, Basic Operation and Analysis, Noise in Switched-Capacitor Circuits, First-Order Filters, Biquad Filters, Charge Injection and Switched-Capacitor Gain Circuits.

UNIT IV

DATA CONVERTERS: Quantization Noise, Signed Codes, Decoder-Based D/A Converters, Binary-Scaled D/A Converters, Thermometer-Code D/A Converters and Hybrid D/A Converters Successive-Approximation A/D Converters, Algorithmic (or Cyclic) A/D Converter, Pipelined A/D Converters, Flash Converters, Two-Step A/D Converters, Interpolating A/D Converters and Folding A/D Converters.

UNIT V

OVERSAMPLING CONVERTERS AND FILTERS: Oversampling without Noise Shaping, Oversampling with Noise Shaping, System Architectures, Digital Decimation Filters, Higher-Order Modulators, Bandpass Oversampling Converters and Practical Considerations.

TEXT BOOKS:

1. Tony Chan Carusone, David A. Johns & Ken Martin, "Analog Integrated Circuit Design",2nd Edition, John Wiley, 2012.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuit" Tata-Mc GrawHill, 2006.

REFERENCES:

1. Philip Allen & Douglas Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2006.
2. Gregolian & Temes, "Analog MOS Integrated Circuits", John Wiley, 2004.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	3	3	3	2	3	3	
CO2	3	3	3	3	2	3	3	
CO3	3	3	3	2	2	3	3	
CO4	3	3	3	3	2	3	3	

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M.Tech- I Semester-VLSI Design

L	T	P	C
3	0	0	3

(20BVL03) DIGITAL IC DESIGN

(ELECTIVE-I)

Outcomes:

On successful completion of the course the student will be able to:

1. Gain knowledge On Layout Design Rules.
2. Solve problems in the design of CMOS logic circuits, with reference to speed and power Consumption.
3. Analyze the static and dynamic characteristics of BICMOS circuits.
4. Design the fundamental blocks of VLSI circuits, both by circuit schematic and physical layout.

UNIT I

CMOS Inverters - Static and Dynamic Characteristics, Static and Dynamic CMOS Design - Domino and NOR Logic - Combinational and Sequential Circuits.

UNIT II

Method of Logical Effort for Transistor Sizing, Power Consumption in CMOS Gates, Arithmetic Circuits in CMOS VLSI – Adders, Multipliers, Shifter.

UNIT III

CMOS Memory Design - SRAM and DRAM, Bipolar Gate Design - BiCMOS Logic - Static and Dynamic Behavior, Delay and Power Consumption in BiCMOS Logic.

UNIT IV

Layout Design Rules: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load**.**

UNIT V

Subsystem Design Process: General arrangement of 4-bit Arithmetic Processor, Design of 4-Bit Shifter, Design of ALU sub-system, Implementing ALU functions with an Adder, Carry-Look-Ahead Adders, Multipliers, Serial Parallel Multipliers, Pipeline Multiplier Array, Modified Booth's Algorithm.

TEXT BOOKS:

1. Jan M Rabaey, "Digital Integrated Circuits - A Design Perspective", Prentice Hall, 2016.
2. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis & Design", MGH, Third Ed., 2002.
3. Douglas A. Pucknell and Kamran Eshraghian, "Basic VLSI Design", PHI, 2013.

REFERENCES:

1. Ken Martin, "Digital Integrated Circuit Design", Oxford University Press, 2000.
2. Neil H E West and Kamran Eshranghian, "Principles of CMOS VLSI Design: A System Perspective", Addision-Wesley 2nd Edition,2002.
3. R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS circuit design, layout, and simulation". New York: IEEE Press, 1998.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	3	2	3	3	1	3	2
CO2	3	3	1	3	3	3	3	2
CO3	2	2	3	1	1	1	3	2
CO4	3	3	3	3	3	1	3	2

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M.Tech- I Semester-VLSI Design

L	T	P	C
3	0	0	3

(20BVL04) VLSI FOR WIRELESS COMMUNICATION (ELECTIVE-I)

Outcomes:
On successful completion of the course the student will be able to
1. Gain knowledge of different modulation schemes.
2. Understand different receiver architecture and low noise amplifier analysis.
3. Analyze the various analog to digital converters.
4. Understand about spread spectrum techniques.

UNIT I

INTRODUCTION: Review of Modulation Schemes – BFSK- BPSK –QPSK – OQPSK – Classical Channel - Additive White Gaussian Noise – Finite Channel Bandwidth - Wireless Channel- Path Environment - Path Loss – Friis Equation – Multipath Fading – Channel Model - Envelope Fading – Frequency Selective Fading – Fast Fading - Comparison of different types of Fading.

UNIT II

RECEIVER ARCHITECTURES : Receiver Front End – Motivations - General Design Philosophy- Heterodyne and Other architectures – Filter Design - Band Selection Filter – Image rejection Filter - Channel Filter - Non idealities and Design Parameters - Harmonic Distortion – Inter modulation -Cascaded Nonlinear Stages – Gain Compression – Blocking – Noise – Noise Sources –Noise Figure - Design of Front end parameter for DECT.

UNIT III

LOW NOISE AMPLIFIER: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching –Power matching – Salient features of LNA – Core Amplifier Design. Active Mixer – Balancing – Gilbert Mixer – Analysis – Noise – Complete Active mixer

UNIT IV

ANALOG TO DIGITAL CONVERTERS: Demodulators - Delta Modulators - Low Pass Sigma Delta Modulators – High Order Modulators - One Bit DAC and ADC –Passive Low Pass Sigma Delta Modulator - Band pass Sigma Delta Modulators – Comparison – PLL based Frequency Synthesizer - Loop Filter Design and Implementation.

UNIT V

SPREAD SPECTRUM: Review of Spread Spectrum – DSSS – FHSS - Basic Principle of DSSS - Modulation –Demodulation-Performance in the presence of noise-narrowband and wideband interferences.Implementations: VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System - Efficient VLSI Architecture for Base Band Signal processing.

TEXT BOOKS:

1. Bosco Leung " VLSI for wireless Communication", Prentice Hall, 2002.
2. Andreas F.Molisch " Wideband wireless Digital Communication", Prentice Hall PTR, 2001.

REFERENCES:

1. George.V.Tsoulous "Adaptive Antennas for wireless Communication", IEEE Press, 2001.
2. Xiaodong Wang and H.Vincent "Wireless Communication System, Advanced Techniques for signal Reception",PearsonEducation. 2004.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	2	1	3	3	2	1	
CO2	3	2	1	3	2	2	1	
CO3	3	2	2	3	2	2	3	
CO4	3	2	3	3	2	2	2	

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M.Tech- I Semester- VLSI Design	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(20BVL05) HARDWARE SOFTWARE CO - DESIGN

(ELECTIVE-I)

Outcomes:

On successful completion of the course the student will be able to

1. Design environment that helps the reader to perform experiments in hardware/software code sign.
2. Understand partition a system into hardware and software components by using techniques
3. Understand various system level specifications
4. Understand design Issues, Trends, and Considerations

UNIT I

CO-DESIGN ISSUES: Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

CO-SYNTHESIS ALGORITHMS: Hardware Software Synthesis Algorithms: Hardware- Software Partitioning, Distributed System Co-Synthesis.

UNIT II

PROTOTYPING AND EMULATION: Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping.

TARGET ARCHITECTURES: Architecture Specialization Techniques, System Communication Infrastructure, Target Architecture and Application System Classes, Architecture for Control Dominated Systems (8051-Architectures for High Performance Control), Architecture for Data Dominated Systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT III

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern Embedded Architectures, Embedded Software Development Needs, Compilation Technologies, Practical Consideration in a Compiler Development Environment.

UNIT IV

DESIGN SPECIFICATION AND VERIFICATION: Design, Co-Design, the Co-Design Computational Model, Concurrency Coordinating Concurrent Computations, Interfacing Components, Design Verification, Implementation Verification, Verification Tools and Interface Verification

UNIT V

LANGUAGES FOR SYSTEM- LEVEL SPECIFICATION AND DESIGN-I: System – Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages,

LANGUAGES FOR SYSTEM-LEVEL SPECIFICATION AND DESIGN-II: Heterogeneous Specifications and Multi Language Co-Simulation, the Cosyma System and LycosSystem.

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Wolf,"Hardware / Software Co- Design Principles and Practice", 2009, Springer.
2. Kluwer , "Hardware / Software Co- Design Principles and Practice", 2002, Academic Publishers.

REFERENCE BOOK:

1. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co-design", 2010, Springer.
2. Giovanni, Wayne Wolf, "Readings in Hardware Software Co – design", Academic Press,2002.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	2	3	2	3	1	1	2
CO2	3	2	2	2	3	2	2	2
CO3	3	2	3	2	2	1	1	2
CO4	3	2	2	2	2	2	2	2

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M.Tech- I Semester-VLSI Design

L	T	P	C
3	0	0	3

(20BVL06) EMBEDDED SYSTEM DESIGN

(ELECTIVE-II)

Outcomes:

On successful completion of the course the student will be able to

1. Perform system analysis and architecture design
2. Apply embedded concepts on real time applications
3. Get Knowledge on ARM processor and SHARC processor
4. Get Knowledge about Debugging techniques

UNIT I

INTRODUCTION: Embedded System Overview, Embedded Hardware Units, Embedded Software in a System, Embedded System on Chip (SoC), Design Process, Classification of Embedded Systems.

EMBEDDED COMPUTING PLATFORM: CPU Bus, Memory Devices, Component Interfacing, Networks for Embedded Systems, Communication Interfacings: RS232/UART, RS422/RS485, IEEE 488 Bus.

UNIT II

SURVEY OF SOFTWARE ARCHITECTURE: Round Robin, Round Robin with Interrupts, Function Queue Scheduling Architecture, Selecting an Architecture Saving Memory Space.

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and Target Machines, Linkers, Locations for Embedded Software, Getting Embedded Software into Target System, Debugging Technique.

UNIT III

RTOS CONCEPTS: Architecture of the Kernel, Interrupt Service Routines, Semaphores, Message Queues, Pipes.

UNIT IV

INSTRUCTION SETS; Introduction, Preliminaries:-Computer Architecture Taxonomy, Assembly Language, ARM Processor:- Processor and Memory Organization, Data Operations, Flow of Control, SHARC Processor**.**

UNIT V

SYSTEM DESIGN TECHNIQUES: Design Methodologies, Requirement Analysis, Specifications, System Analysis and Architecture Design.

DESIGN EXAMPLES: Telephone PBX, Ink Jet Printer, Water Tank Monitoring System, GPRS, Personal Digital Assistants, Set Top boxes.

TEXT BOOKS:

1. Wayne Wolf, "Computers as a Component: Principles of Embedded Computing System Design", 2nd Edition, 1998.
2. David E, Simon, " An Embedded Software", Premier
3. KVKK Prasad, "Embedded / Real Time Systems", Dreamtech Press, 2005

REFERENCES:

1. Sri Ram V Iyer, Pankaj Gupta, "Embedded Real Time Systems Programming", TMH, 2004
2. Frank Vahid, Tony D.Givargis, "Embedded System Design- A Unified Hardware/Software Introduction", John Willey, 2002.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	2	2	1	3		3	2	
CO2	2	2	1			3	2	
CO3	2	3	3	3		3	2	
CO4	2	2	1			3	2	

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M.Tech- I Semester-VLSI Design

L	T	P	C
3	0	0	3

(20BVL07) HARDWARE DESCRIPTION LANGUAGES
(ELECTIVE-II)

Outcomes:

On successful completion of the course the student will be able to

1. Analyze the various design methodologies in HDL.
2. Program in verilog HDL for digital circuits.
3. Analyze the synthesis of digital circuits.
4. Design the digital circuits in verilog HDL.

UNIT I

HARDWARE MODELING WITH THE VERILOG HDL : Hardware Encapsulation, Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers.

UNIT II

LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOG HDL: User-Defined Primitives, Combinational Behavior User-Defined Primitives, Sequential Behavior User-Defined Primitives, Initialization of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings. Constants, Operators, Expressions and Operands, Operator Precedence Models of Propagation Delay, Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

UNIT III

BEHAVIORAL DESCRIPTIONS IN VERILOG HDL: Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.

UNIT IV

SYNTHESIS OF COMBINATIONAL LOGIC: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Three State Outputs and Don't Cares, Synthesis of Sequential Logic Synthesis of Sequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets, Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.

SYNTHESIS OF LANGUAGE CONSTRUCTS: Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-Defined Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

UNIT V

SWITCH-LEVEL MODELS IN VERILOG: MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic, Design Examples in Verilog.

TEXT BOOKS:

1. M.D.Ciletti, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", Prentice-Hall, 1999.
2. Z.Nawabi, "VHDL Analysis and Modeling of Digital Systems", (2/E), McGraw Hill, 1998.

REFERENCES:

1. M.G.Arnold, "Verilog Digital – Computer Design", Prentice-Hall (PTR), 1999.
2. Perry, "VHDL", (3/E), McGraw Hill.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	3	1	2	3	3	3	3
CO2	3	3	2	2	3	3	3	3
CO3	3	3	3	3	3	3	3	3
CO4	3	3	1	3	3	3	3	3

Sri Venkateswara College of Engineering and Technology, Chittoor. (Autonomous)

M.Tech-I Semester- VLSI Design

L	T	P	C
3	0	0	3

(20BVL08) IMAGE PROCESSING AND PATTERN RECOGNITION

(ELECTIVE- II)

Outcomes:

On successful completion of the course the student will be able to

1. Describe and explain the general processes of image acquisition and storage.
2. Understand enhancement, segmentation, representation, and description.
3. Implement filtering and enhancement algorithms for monochrome as well as color images.
4. Design and implement visual pattern recognition solutions.

UNIT I

IMAGE REPRESENTATION: Gray Scale and Colour Images, Image Sampling and Quantization. Two Dimensional Orthogonal Transforms: DFT, WHT, Haar Transform, KLT, DCT.

UNIT II

IMAGE ENHANCEMENT: Filters in Spatial and Frequency Domains, Histogram-Based Processing, Homomorphic Filtering. Edge Detection, Non Parametric and Model based Approaches, LOG Filters, Localization Problem.

IMAGE RESTORATION: Degradation Models, PSF, Circulant and Block - Circulant Matrices, Deconvolution, Restoration using Inverse Filtering, Wiener Filtering and Maximum Entropy based Methods.

UNIT III

IMAGE SEGMENTATION: Pixel Classification, Bi-Level Thresholding, Multi-Level Thresholding, P-Tile Method, Adaptive Thresholding, Spectral & Spatial Classification, Edge Detection, Hough Transform, Region Growing.

FUNDAMENTAL CONCEPTS OF IMAGE COMPRESSION: Compression models, Information theoretic perspective, Fundamental coding theorem.

UNIT IV

INTRODUCTION: Machine Perception Pattern Recognition Example, Pattern Recognition Systems, Design Cycle, Learning and Adaption.

BAYESIAN DECISION THEORY: Introduction, Continuous Features, Two Categories Classifications, Minimum Error Rate Classification, Zone-One Loss Function, Classifiers, Discriminate Functions and Decision Surfaces.

UNIT V

NORMAL DENSITY: Univariate and Multivariate Density, Discriminant Functions For The Normal Density Different Cases, Bayes Decision Theory – Discrete Features, Compound Bayesian Decision Theory and Context.

MAXIMUM LIKELIHOOD AND BAYESIAN PARAMETER ESTIMATION: Introduction, Maximum Likelihood Estimation, Bayesian Estimation, Bayesian Parameter Estimation – Gaussian Case.

TEXT BOOKS

1.R. C. Gonzalez, R. E. Woods, "Digital Image Processing", Pearson Education. 2nd Edition,2002

2. Richard O. Duda, Peter E. hart, David G. Stroke, "Pattern classifications", Wiley student Edition, Second Edition.

3. Sergios Theodoridis and Knostantinos koutroumbas, "Pattern Recognition", Third Edition, Academic Press.

REFERENCES:

1. S Jayaraman, S Esakkirajan, T Veerakumar, "Digital Image processing", Tata McGrawHill
2. R. Jain, R. Kasturi and B.G. Schunck, "Machine Vision", McGraw-Hill International Edition, 1995
3. Lawerence Rabiner, Biing – Hwang Juang, "Fundamentals of Speech Recognition", Pearson Education.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1		2				2	1	3
CO2	2	2		2		2	1	3
CO3	2	2		2		2	1	3
CO4	2	2		2		2	1	3

SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY
(AUTONOMOUS)
(20BMB21) RESEARCH METHODOLOGY

I M.Tech I Semester

L	T	P	C
2	0	0	2

OUTCOMES*:*

After completion of the course, the students will be able to:

1. Explain the concepts, objectives, and process of research (Understanding).
2. Formulate the research problem and develop a sufficiently coherent research design (Creating).
3. Identify the measuring and scaling procedure used in research (Applying).
4. Use statistical tools for descriptive and inferential analysis (Applying).
5. Outline the key elements of report writing (Remembering).

Unit-I: Research:Meaning, Objective, Motivation in Research, Types of Research, Research Approaches, Research Process; Validity and Reliability in Research; Research Design: Features of Good Design, Types of Research Design, and Basic Principles of Experimental Design.

Unit-II: Sampling Design: Meaning ,Steps in Sampling Design, Characteristics of a Good Sample Design, Random Samples and Random Sampling Design; Measurement and Scaling Techniques: Errors in Measurement, Tests of Sound Measurement, Scaling and Scale Construction techniques, Forecasting Techniques, Time Series Analysis, Interpolation and Extrapolation.

Unit-III: Methods of Data Collection: Primary Data, Questionnaire and Interviews, Collection of Secondary Data, Cases and Schedules. Professional Attitude and Goals, Concept of Research Excellence, Ethics in Science and Engineering, Frauds in Science and Research.

Unit-VI: Correlation and Regression Analysis, Method of Least Squares, Regression Vs. Correlation, Correlation Vs. Determination, Types of Correlation and Their Specific Applications; Statistical Interference: Tests of Hypothesis, Parametric Vs. Non-Parametric Tests, Procedure for Testing Hypothesis, Use Statistical Techniques for Testing Hypothesis, Sampling Distribution, Sampling T Chi-Square Test, Analysis of Variance and Covariance, Multivariable Analysis

Unit V: interpretation of Data and Report Writing, Layout of a Research Paper, Techniques of Interpretation, Making Scientific Presentation at Conferences and Popular Lectures to Semi Technical Audience, Participating in Public Debates on Scientific Issues.

TEXT BOOKS:

1. Garg, C. K. (2019). Research Methodology: Methods And Techniques (4 ed.). New Delhi: New Age International Publisher.
2. Bhattacharyya, D. K. (2006). Research Methodology (2 ed.). New Delhi: Excel Books.
3. O.R.Krishnaswamy and D.Obul Reddy,(2009),Research Methodology and Statistical Analysis, Himalaya Publication,(2nd Edition)

MAPPING COs WITH POs:

COURSE OUTCOMES	PROGRAM OUTCOMES										
	1	2	3	4	5	6	7	8	9	10	11
CO1				2	3					1	
CO2				2	3					2	
CO3					3					2	
CO4				2	3					1	
CO5				2	2						
3- High Mapping				2-Medium Mapping						1- Low Mapping	

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M.Tech- I Semester-VLSI Design

L	T	P	C
0	0	4	2

(20BVL09) DIGITAL SYSTEM DESIGN LAB

Course Outcome:

On successful completion of the course the student will be able to

1. Different modeling styles available in VHDL and Verilog and difference between them
2. Difference between verilog and VHDL
3. Representation of different digital modules in different modelling styles available in VHDL and Verilog.

Using VHDL or Verilog do the following experiments

1. Design of 4-bit adder / subtractor
2. Design of Booth Multiplier
3. Design of 4-bit ALU
4. Design SISO, SIPO, PISO, PIPO Registers
5. Design of Ripple, Johnson and Ring counters
6. Design of MIPS processor
7. Design of Washing machine controller
8. Design of Traffic Light Controller
9. Design “1010” pattern detector using Mealy state Machine
10. Design “1100” recursive pattern detector using Moore state Machine
11. Design simple Security System Using FSM/ASM
12. Mini Project

Tools Required:

VHDL or VERILOG

Hardware Required:

Computers with latest Configuration.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	2					3	1	2
CO2	2	1				3	1	2
CO3	2	2		2	2	3	1	2

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M.Tech- I Semester-VLSI Design

	L	T	P	C
(20BVL10) VLSI SYSTEM DESIGN LAB	**0**	**0**	**4**	**2**

Outcomes:

On successful completion of the course the student will be able to

1.Understand syntax of various commands available with verilog and fundamental associated with design of digital systems

2. Design and simulate and implement various digital system like traffic light controller, UART.

3. Develop problem solving skills and adapt them to solve real world problems

4. Develop scripts using perl for building digital blocks

The students are required to design the logic circuit to perform the following experiments using necessary simulator (Xilinx ISE Simulator/Mentor Graphics Questa Simulator) to verify the logical /functional operation and to perform the analysis with appropriate synthesizer (Xilinx ISE Synthesizer/Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).

The students are required to design and implement the Layout of the following experiments of any SIX using CMOS 130nm Technology.

List of Experiments:

1. Inverter Characteristics.
2. Full Adder.
3. RS-Latch, D-Latch and Clock Divider.
4. Synchronous Counter and Asynchronous Counter.
5. Static RAM Cell.
6. Dynamic RAM Cell.
7. ROM
8. Digital-to-Analog-Converter.
9. Analog-to-Digital Converter.
10. “10101” pattern detector using Mealy FSM
11. Analytical Comparator.
12. Mini Project

Lab Requirements:

Software:

Xilinx ISE Suite, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Perl Software.

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	3	2	3	2	3	3	3
CO2	3	3	2	2	2	3	3	3

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M.Tech – I Semester – VLSI Design

L	T	P	C
2	0	0	0

(20BVL11) HUMAN VALUES AND PROFESSIONAL ETHICS (Audit Course)

Outcomes:

On successful completion of the course the student will be able to

1. Understand the importance of human values and ethics.
2. Understand engineer ethics related to various theories.
3. Understand about social experimentation as well as safety and risky analysis.
4. Understand various global issues and computer ethics.

Unit I:

HUMAN VALUES:Morals, Values and Ethics-Integrity-Work Ethic-Service learning – Civic Virtue – Respect for others – Living Peacefully – Caring – Sharing – Honesty - Courage- Co Operation – Commitment – Empathy –Self Confidence Character – Spirituality.

Unit II:

ENGINEERING ETHICS: Senses of Engineering Ethics- Variety of moral issues – Types of inquiry – Moral dilemmas – Moral autonomy –Kohlberg‟s theory- Gilligan‟s theory- Consensus and controversy – Models of professional roles- Theories about right action- Self interest -Customs and religion –Uses of Ethical theories – Valuing time –Co operation – Commitment.

Unit III :

ENGINEERING AS SOCIAL EXPERIMENTATION: Engineering As Social Experimentation – Framing the problem – Determining the facts – Codes of Ethics – Clarifying Concepts – Application issues – Common Ground - General Principles – Utilitarian thinking respect for persons.

UNIT IV:

ENGINEERS RESPONSIBILITY FOR SAFETY AND RISK: Safety and risk – Assessment of safety and risk – Risk benefit analysis and reducing riskSafety and the Engineer- Designing for the safety- Intellectual Property rights(IPR).

UINIT V:

GLOBAL ISSUES: Globalization – Cross culture issues- Environmental Ethics – Computer Ethics – Computers as the instrument of Unethical behavior – Computers as the object of Unethical acts – Autonomous Computers- Computer codes of Ethics – Weapons Development - Ethics .

Text Books :

1. “Engineering Ethics includes Human Values” by M.Govindarajan, S.Natarajan and V.S.SenthilKumar- PHI Learning Pvt. Ltd-2009.
2. “Engineering Ethics” by Harris, Pritchard and Rabins, CENGAGE Learning, India Edition, 2009.
3. “Ethics in Engineering” by Mike W. Martin and Roland Schinzinger – Tata McGrawHill–2003.
4. “Professional Ethics and Morals” by Prof.A.R.Aryasri, Dharanikota Suyodhana-Maruthi Publications.
5. “Professional Ethics and Human Values” by A.Alavudeen, R.Kalil Rahman and M.Jayakumaran , Laxmi Publications.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1						1		
CO2						1		
CO3						2		
CO4						3		

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M.Tech- II Semester-VLSI Design

L	T	P	C
3	0	0	3

(20BVL12) LOW POWER VLSI DESIGN

Outcomes:

On successful completion of the course the student will be able to

1. Know the Low-Power Design Approaches.
2. Analyze the Standard Adder Cells, CMOS Adder's Architectures.
3. Understand the operation of Low-Voltage Low-PowerMemories.
4. Understand the Switched Capacitance Minimization Approaches.

UNIT –I

FUNDAMENTALS: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II

LOW-POWER DESIGN APPROACHES: Low-Power Design through Voltage Scaling **–** VTCMOS Circuits, MTCMOS Circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

SWITCHED CAPACITANCE MINIMIZATION APPROACHES: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III

LOW-VOLTAGE LOW-POWER ADDERS: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV

LOW-VOLTAGE LOW-POWER MULTIPLIERS: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier, Gilbert's Multiplier.

UNIT –V

LOW-VOLTAGE LOW-POWER MEMORIES: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Pre-charge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits – Analysis and Design", TMH, 2011.
2. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems", TMH Professional Engineering.

REFERENCE BOOKS:

1. Anantha Chandrakasan, "Low Power CMOS Design", IEEE Press/Wiley International, 1998.
2. Kaushik Roy, Sharat C. Prasad ,"Low Power CMOS VLSI Circuit Design", John Wiley & Sons, 2000.
3. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Press, 2002.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	3	2	3	3	3		
CO2	3	3	2	2	2	3		
CO3	3	3	3	3	2	3		
CO4	3	3	3	3	2	3		

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L	T	P	C
3	0	0	3

(20BVL18) ELECTRONIC DESIGN AUTOMATION TOOLS
(ELECTIVE-IV)

Outcomes:

On successful completion of the course the student will be able to

1. Understand about Leonardo spectrum, ISE 8.1i, Quartus II, VLSI backend tools.
2. Understand about Synthesis and simulation using HDLs.
3. Design about Various Circuit simulation using Spice 4.Classical hardware modeling in system C

UNIT I

An Overview of OS Commands. System Settings and Configuration, Introduction to Unix Commands, Writing Shell Scripts, VLSI Design Automation Tools, An Overview of the features of Practical CAD Tools. Modelsim, Leonardo Spectrum, ISE 8.1i, Quartus II, VLSI Backend Tools.

UNIT II

Synthesis using HDLs-Logic Synthesis using Verilog and VHDL, Memory and FSM Synthesis, Performance Driven Synthesis,

UNIT III

Simulation, Types of Simulation, Static Timing Analysis, Formal Verification, Switch Level and Transistor Level Simulation.

UNIT IV

Circuit Simulation using Spice - Circuit Description. AC, DC and Transient Analysis, Advanced Spice Commands and Analysis, Models for Diodes, Transistors and Opamp, Digital Building Blocks, A/D, D/A and Sample and Hold Circuits, Design and Analysis of Mixed Signal Circuits.
Mixed Signal Circuit Modeling and Analysis using VHDL–AMS.

UNIT V

System Design Using SystemC- SystemC Models of Computation, Classical Hardware Modeling in System C. Functional Modeling, Parametrized Modules and Channels, Test Benches, Tracing and Debugging.

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	L	T	P	C
M.Tech- II Semester-VLSI Design	**3**	**0**	**0**	**3**

(20BVL13) ALGORITHMS FOR VLSI DESIGN AUTOMATION

Outcomes:

On successful completion of the course the student will be able to

1. Gain knowledge on various design methodologies and design automation tools.
2. Understand the different search algorithms.
3. Understand the modeling and simulation.
4. Understand the logic synthesis.

UNIT I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable problems.

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III

LAYOUT AND PLACEMENTS: Layout Compaction, Placement, Floor Planning And Routing Problems, Concepts and Algorithms.

UNIT IV

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch Level Modeling and Simulation.

LOGIC SYNTHESIS AND VERIFICATION: Basic Issues and Terminology, Binary-Decision Diagrams, Two-Level Logic Synthesis

HIGH-LEVEL SYNTHESIS: Hardware Models, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment Problem, High-level Transformations.

UNIT V

PHYSICAL DESIGN AUTOMATION OF FPGAs: FPGA technologies, Physical Design Cycle for FPGA's, Partitioning and Routing for Segmented and Staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCMs: MCM technologies, MCM physical design cycle, Partitioning, Placement- Chip Array based and Full Custom Approaches,

Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin, Distribution and routing, Routing and Programmable MCM's.

TEXTBOOKS:

1. S.H.Gerez, "Algorithms for VLSI Design Automation", WILEY Student Edition, John Wiley & Sons , 2002.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd Edition, Springer International Edition, 2005.

REFERENCES:

1. Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", Wiley, 1993.
2. Wayne Wolf, "Modern VLSI Design Systems on Silicon", Pearson Education Asia, 2nd Edition, 1998.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	3	2	2	3	3	3	3
CO2	3	3	3	3	3	3	3	
CO3	3	3	3	3	3	3	3	3
CO4	3	3	3	3	3	3	3	3

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L	T	P	C
3	0	0	3

(20BVL14) NANO ELECTRONICS

(ELECTIVE- III)

Outcomes:

On successful completion of the course the student will be able to

1. Understand various methods to fabricate.
2. Analyze nanoscale features
3. Get knowledge on mass storage device
4. Understand data transmission

UNIT I

NANO TECHNOLOGY AND SCIENCE: Introduction, Nano Film Deposition Techniques, Magnetron Sputtering, Laser Ablation, Molecular Beam Epitaxy Deposition, Lithography, Material Removing Technologies, Chemical Etching , Mechanical Processing, Scanning Probe Techniques. Carbon Nano Structures: C_{60} and Fullerence, Carbon Nano Tubes, Fabrication, Electrical, Mechanical and Vibrational Properties, Applications of Carbon Nano Tubes.

UNIT II

LOGIC DEVICES: Silicon MOSFETs, Novel Materials and Alternative Concepts, Ferro Electric Filed Effect Transistors, Super Conductor Digital Electronics, Carbon Nano Tubes for Data Processing.

UNIT III

RADOM ACESS MEMORIES: High Permittivity Materials for DRAMs, Ferro Electric Random Access Memories, Magneto-Resistive RAM.

UNIT IV

MASS STORAGE DEVICES:

Hard Disk Drives, Magneto Optical Disks, Rewriteable DVDs based on Phase Change Materials, Holographic Data Storage.

UNIT V

DATA TRANSIMISSION, INTERFACES AND DISPLAYS:

Photonic Networks, Microwave Communication Systems, Liquid Crystal Displays, Organic Light Emitting Diodes.

TEXTBOOKS:

1. Rainer Waser, "Nano Electronics and Information Technology", WileyVCH, April 2003.
2. Charles Poole, "Introduction to Nano Technology", Wiley Interscience, May 2003.

REFERENCE BOOKS:

1. George W. Hanson, "Fundamentals of Nano Electronics", 2009.
2. Mitin, "Introduction To Nano electronics Science, Nanotechnology, Engineering, And Applications", 2010.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	3	2	3	2	3	3	
CO2	3	3	3	3	3	3	3	
CO3	3	3	2	3	1	3	3	
CO4	3	3	3	3	3	3	3	

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L	T	P	C
3	0	0	3

20BCS13CRYPTOGRAPHY AND NETWORK SECURITY

(Elective- III)

Course Outcomes:

On successful completion of the course the student will be able to

1. Apply various classical encryption techniques for real time application
2. Compare various Cryptographic Techniques
3. Design Secure applications
4. Apply secure coding in the developed applications

UNIT I

Introduction and Modern Techniques

Attacks - Services and mechanisms - Security attacks - Security services - A Model for network security - Classical encryption techniques - Symmetric cipher model – Substitution techniques – Transposition techniques – Rotor machines – Steganography.

Modern Techniques: Simplified DES - Block cipher principles - Data Encryption Standard - Strength of DES - Differential and linear cryptanalysis - Block Cipher Design Principles

UNIT II

Conventional Encryption and Public Key Cryptography and Hash and Mac Algorithms

Confidentiality Using Symmetric Encryption: Placement of encryption function - Traffic confidentiality - Key distribution - Random Number Generation-**Public Key Cryptography:** Principles - RSA Algorithm - Key management - Diffie- Hellman key exchange-**Hash and Mac Algorithms:** Secure hash algorithm – Whirlpool – HMAC - CMAC

UNIT III

Digital signatures, Authentication protocols and Authentication Applications

Digital signatures - Authentication protocols - Digital signature standard -**Authentication Applications:** Kerberos - X.509 Authentication service – Public key infrastructure

UNIT IV

Electronic Mail Security and IP Security

Electronic Mail Security -Pretty Good Privacy - S/MIME -IP Security: Overview - Architecture – Authentication header - Encapsulating security Payload - Combining security associations - Key

management

UNIT V

Web Security and Intruders

Web Security Considerations - Secure socket layer and transport layer security - Secure Electronic Transaction - **Intruders:** Intruders - Intrusion detection - Password management – Firewalls - Firewall design principles - Trusted systems

TEXT BOOKS:

1. "Cryptography and Network Security", 4/e, 2006, William Stallings , Pearson Education, New Delhi ,India.
2. "Network Security Essentials (Applications and Standards)", 3/e, 2007, William Stallings, Pearson Education, New Delhi, India.

REFERENCE BOOKS:

1. "Security in Computing", 4/e, 2009, Charles P. Pfleeger, Shari Lawrence Pfleeger, Deven Shah, Pearson Education, New Delhi, India.
2. "Principles and Practices of Information Security", 4/e, 2012, Michal E. Whitman and Herbert J. Mattord, Cengage Learning, New Delhi.

3-

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	**2**	**3**					**1**						**2**	
CO2	**3**												**2**	
CO3		**3**											**2**	
CO4			**2**	**1**							**1**			**3**

High mapping **2-Medium Mapping** **1- Low Mapping**

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M.Tech – II Semester- VLSI Design

L	T	P	C
3	0	0	3

(20BVL15) SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION (ELECTIVE-III)

Outcomes:

On successful completion of the course the student will be able to

1. Gain the innovative ideas to develop a Static web Document
2. Develop a dynamic web Documents using XML and CSS
3. Gain the Reporting and Designing knowledge
4. Apply the Programming skills and Activities

UNIT I:

Overview of Scripting Languages, HTML, Basic Tags, List, Tables, Images, Forms, Frames, CSS.

UNIT II: Introduction to Java Scripts**,** Objects in Java Script, Dynamic HTML with Java Script XML : Document type definition , XML Schemas, Document Object model , Using Xml Processors, DOM and SAX

UNIT III: PERL: Operators, Statements, Pattern Matching, Modules, Objects , Variables , Constants ,Conditionals, Loops, Regular Expressions , Manipulation of Data Structures Function with Programming Examples.

UNIT IV: Interprocess Communication Threads, Compilation & Line Interfacing, Debugger Internal & Externals Portable Functions.

UNIT V: Basic Programming with Example of HTML, JavaScript, XML, Perl.

TEXT BOOKS :

1. Dietel and Nieto, “Internet and World wide web–How to program”, Pearson Education.
2. Patrick Naughton and Herbert Schildt, “The complete Reference java-2”, Third Edition

REFERENCES :

1. Wang, “An Introduction to web Design and Programming”, ThomsonEdition
2. Sebesta , “Programming world wide web”, Pearson Edition

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	2		3	1	3		2	
CO2	2		3	1	3		2	
CO3	2	2	3	1	3		2	
CO4	2		3	1	3		2	

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L	T	P	C
3	0	0	3

M.Tech-II Semester- VLSI Design

(20BVL16) DSP PROCESSORS AND ARCHITECTURES
(ELECTIVE – IV)

Outcomes:

On successful completion of the course the student will be able to

1. Understand about DSP Processors- TMS320C544XX.
2. Understand about Implementation of basic DSP algorithms using DSP Processors.
3. Understand Various bus architectures and memory
4. Understand Memory interfacing to Programmable DSP devices

UNIT-I

INTRODUCTION TO DIGITAL SIGNAL PROCESSING: Introduction, A Digital Signal-Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time Invariant Systems, Digital Filters, Decimation and Interpolation.

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS: Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementations, A/D Conversion Errors, DSP Computational Errors, D/A Conversion Errors, Compensating Filter.

UNIT-II

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

EXECUTION CONTROL AND PIPELINING: Hardware Looping, Interrupts, Stacks, Relative Branch Support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching Effects, Interrupt Effects, Pipeline Programming Models.

UNIT-III

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Commercial Digital Signal-Processing Devices, Data Addressing modes of TMS320C54XX Processors, Memory space, Program Control, Instructions and Programming, On-Chip Peripherals, Interrupts and Pipeline Operation of TMS320C54XX Processors.

UNIT-IV

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing. An FFT Algorithm for DFT Computation, Butterfly Computation, Overflow and Scaling, Bit- Reversed Index Generation, An 8-Point FFT Implementation on the TMS320C54XX, Computation of the Signal Spectrum.

UNIT-V

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES:

Memory Space Organization, External Bus Interfacing Signals, Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O, Direct Memory Access (DMA). A Multi-Channel Buffered Serial Port (MCBSP), MCBSP Programming, COURSE CODEC Interface Circuit, COURSE CODEC Programming, COURSE CODEC-DSP Interface Example.

TEXT BOOKS:

1. Avtar Singh and S. Srinivasan, "Digital Signal Processing", Thomson Publications,2004.
2. Lapsley et al, "DSP Processor Fundamentals, Architectures & Features", S. Chand & Co, 2000.

REFERENCES:

1. Jonathan Stein, "Digital Signal Processing", John Wiley, 2005.
2. B. Venkata Ramani and M. Bhaskar, "Digital Signal Processors, Architecture, Programming and Applications", TMH, 2004.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	2	3	1	3	1	2	3	
CO2	2	3	2	3	1	2	3	
CO3	2	3	3	3	1	2	3	
CO4	2	3	3	3	1	2	3	

Sri Venkateswara College of Engineering and Technology, Chittoor.
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M.Tech- II Semester- VLSI Design

L	T	P	C
3	0	0	3

(20BVL17) DESIGN OF SEMICONDUCTOR MEMORIES

Outcomes:
On successful completion of the course the student will be able to
1. Gain knowledge of different Random Access and Non volatile Memory.
2. Understand about advanced memory technologies.
3. Understand about semiconductor memory reliability and radiation effects.
4. Gain knowledge about fault modeling and testing.

UNIT I

RANDOM ACCESS MEMORY TECHNOLOGIES: Static Random Access Memory(SRAMs):SRAM cell structure-MOS SRAM architecture-MOS SRAM cell and peripheralcircuit operation-bipolar SRAM technologies- Silicon on insulator(SOI) technology-advanced SRAM architectures and technologies, application specific SRAMs-CMOS CRAMs - DRAMs cell theory and advanced cell structures-BiCMOSDRAMs-soft error failure in DRAMs - Advanced DRAM designs and architecture-application specific DRAMs.

UNIT II

NONVOLATILE MEMORIES: Masked Read-only memories (ROMs):High density ROMs-Programmable read only memories(PROMs) – Bipolar PROMs- CMOS PROMs-erasable (UV)-Programmable read only memories (EPROMs)-Floating Gate EPROMcell-one -time programmable (OTP) EPROMs-Electrically Erasable PROMs(EEPROMs)- EEPROM technology andarchitecture – non-volatile SRAM-Flash memories(EPROMs or EEPROM)-Advanced flash memory architecture – Phase Change Memory–Design Techniques of PCM–Magnetoresistive RAM– Resistive RAM.

UNIT III

ADVANCED MEMORY TECHNOLOGIES AND HIGH –DENSITY MEMORY

PACKAGING TECHNOLOGIES: Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog memories magneto resistive random access memories (MRAMs) – Experimental memory devices. Memory hybrids and MCMs (2D)-Memory stacks and MCMs (3D)-Memory MCM testing and reliability issues-memory cards-high density memory packaging future directions.

UNIT IV

SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS: General Reliability issues-RAM failure modes and mechanism-nonvolatile memory reliability-reliability modeling and failure rate prediction- design for reliability-reliability test structures-reliability screening and qualification. Radiationeffects-single event phenomenon (SEP)-radiation hardening techniques-radiation hardening process and design issues-radiation hardened memory characteristics-radiation hardness assurance and testing-radiation dosimetry – waterlevel radiation testing and structures.

UNIT V

MEMORY FAULT MODELING,TESTING AND MEMORY DESIGN FOR TESTABILITY & FAULT TOLERANCE: RAM fault modelling,electrical testing,Pseudo random testing-megabit DRAM- nonvolatile memory modelling and testing-IDDQ fault modelling and testing-application specific memory testing and the tools for fault modelling and testing.

TEXT BOOKS:

1. Ashok K.Sharma “Semiconductor Memories Technology, testing and reliability", IEEE Press, 1st edition, 2002.
2. Ivan Sutherland Bob sproull, David Harris, "Logical Efforts, Designing Fast CMOS Circuits", Kluwr Academic Press, 1999.

REFERENCES:

1. David Harris, "Skew Tolerant domino Design", Prentice Hall of India Private Ltd, 2000
2. Hai Li, “Nonvolatile Memory Design: Magnetic, Resistive, and Phase Chang”,CRC Press, December 19, 2011.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	3	1	1	1	3	3	
CO2	3	3	2	3	1	3	3	
CO3	3	3	3	3	1	3	3	
CO4	3	3	3	3	1	3	3	

TEXT BOOKS:

1. M.J.S.Smith, “Application Specific Integrated Circuits”,Pearson, 2002
2. M.H.Rashid, “Spice for Circuits and Electronics using Pspice”, (2/e), PHI.

REFERENCE BOOKS:

1. T. Grdtker et al , “System Design with System-C”, Kluwer, 2004.
2. P.J. Ashenden et al , “The System Designer’s Guide to VHDL-AMS”, Elsevier,2005

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	3	3	3	3	3	3	3
CO2	3	3	2	3	3	3	3	3
CO3	3	3	2	3	3	3	3	3
CO4	3	3	3	3	3	3	3	3

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M.Tech- II Semester- VLSI Design

L	T	P	C
0	0	4	2

(20BVL19) MINI PROJECT

Sri Venkateswara College of Engineering and Technology, Chittoor. (Autonomous)

M.Tech-II Semester-VLSI Design

L	T	P	C
0	0	4	2

(20BVL20) MIXED SIGNAL LAB

Outcomes:

On successful completion of the course the student will be able to:

1. Design the various schematics and layouts for different circuits.
2. Analyze the importance of DRC.

1. Analog Circuits Simulation using Spice.
2. Mixed Signal Simulation using Mixed Signal Simulators.
3. Layout Extraction for Analog & Mixed Signal Circuits.
4. Parasitic Values Estimation from Layout.
5. Layout Vs Schematic.
6. Net List Extraction.
7. Design Rule Checks.

NOTE: Required Software Tools:

1. Tanner tools /Mentor Graphic tools / Cadence tools/ Synopsystools.
2. Xilinx 9.1i and Above for FPGA/CPLDS.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	3	3	3	3	3	3	3
CO2	3	3	3	3	3	3	3	3

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M.Tech- II Semester-VLSI Design

L	T	P	C
0	0	4	2

(20BVL21) EMBEDDED SYSTEMS LAB

Outcomes:

On successful completion of the course the student will be able to:

1. Perform interfacing using LED &LCD.
2. Perform the program using assembly & C Languages.
3. Perform serial transmission& Reception.

ASSEMBLY:

1. Write a program to

a) Clear the Register

b) Add 3 to Register Ten Times and Place the Result into Memory Use the Indirect Instructions to Perform Looping.

PROGRAMING IN C:

2. A Door Sensor is connected to RB1 Pin and a Buzzer is connected to RB7**.** Write a Program to monitor Door Sensor and when it Open, Sounds the Buzzer by sending a Square Wave of few Hundred Hz Frequency to it.
3. Write a Program to Toggle all the Bits of PORT B parts continuously with a 250ns Delay.
4. LED'S
   (A) Blinking LEDs
   (B) Dancing LEDs
5. LCD Interface
6. Serial Communication
   A) Serial Transmission
   B) Serial Reception

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	2					3	1	2
CO2	2	1				3	1	2
CO3	2	2		2	2	3	1	2

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M.Tech II semester (VLSI SYSTEM DESIGN)

L	T	P	C
2	0	0	0

(20BVL22) INTELLECTUAL PROPERTY RIGHTS (Audit Course)

Outcomes:

On successful completion of the course the student will be able to

1. Know about the types of IPR
2. Understand various trade mark and copy right issues.
3. Understand about trade secret and related issues
4. Gain knowledge about various laws related IPR

UNIT – I

Introduction To Intellectual Property: Introduction, Types Of Intellectual Property, International Organizations, Agencies And Treaties, Importance Of Intellectual Property Rights.

UNIT – II

Trade Marks : Purpose And Function Of Trade Marks, Acquisition Of Trade Mark Rights, Protectable Matter, Selecting And Evaluating Trade Mark, Trade Mark Registration Processes.

UNIT – III

Law Of Copy Rights : Fundamental Of Copy Right Law, Originality Of Material, Rights Of Reproduction, Rights To Perform The Work Publicly, Copy Right Ownership Issues, Copy Right Registration, Notice Of Copy Right, International Copy Right Law.

Law Of Patents : Foundation Of Patent Law, Patent Searching Process, Ownership Rights And Transfer

UNIT – IV

Trade Secrets : Trade Secrete Law, Determination Of Trade Secrete Status, Liability For Misappropriations Of Trade Secrets, Protection For Submission, Trade Secrete Litigation.

Unfair Competition : Misappropriation Right Of Publicity, False Advertising.

UNIT – V

New Development Of Intellectual Property: New Developments In Trade Mark Law ; Copy Right Law, Patent Law, Intellectual Property Audits.

International Overview On Intellectual Property, International – Trade Mark Law, Copy Right Law, International Patent Law, International Development In Trade Secrets Law.

TEXT BOOKS & REFERENCES:

1. Intellectual Property Right, Deborah. E. Bouchoux, Cengage Learing.

2. Intellectual Property Right – Nleashmy The Knowledge Economy, Prabuddha Ganguli, Tate Mc Graw Hill Publishing Company Ltd.,

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1						1		
CO2						1		
CO3						2		
CO4						3		

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M.Tech- III Semester- VLSI Design

L	T	P	C
3	0	0	3

(20BVL23) FPGA ARCHITECTURES & APPLICATIONS
(ELECTIVE-V)

Outcomes:

On successful completion of the course the student will be able to

1. Understand about different commercially available FPGA and CPLD architectures.
2. Design logic blocks using optimization techniques.
3. Understand the top down design of digital circuits.
4. Understand about mentor graphics EDA tool.

UNIT I

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices ALTERA Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice PLSIs Architectures – 3000 Series – Speed Performance and in System Programmability.

UNIT II

Field Programmable Gate Arrays – Logic Blocks, Routing Architecture, Design Flow, Technology Mapping for FPGAs.

CASE STUDIES: XILINX XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and their Speed Performance.

UNIT III

FINITE STATE MACHINES (FSM): Top Down Design, State Transition Table, State Assignments for FPGAs, Problem of Initial State Assignment for One Hot Encoding.

REALIZATION OF STATE MACHINE: Charts with a PAL, Alternative Realization for State Machine Chart using Micro-programming, Linked State Machines. One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties. Extended Petrinetes for Parallel Controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

UNIT IV

FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN: Architectures Centered around Non- Registered PLDs, State Machine Designs Centered around Shift Registers, One – Hot Design Method, Use of ASMs in One – Hot Design, K Application of One – Hot Method, System Level Design – Controller, Data Path and Functional Partition.

UNIT V

DIGITAL FRONT END DIGITAL DESIGN TOOLS FOR FPGAS & ASICS: UsingMentor

Graphics EDA Tool (FPGA Advantage), Design Flow Using FPGAs – Guidelines and Case Studies of Parallel Adder Cell, Parallel Adder Sequential Circuits, Counters, Multiplexers, Parallel Controllers.

TEXT BOOKS:

1. P.K.Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Prentice Hall , 1994.
2. Stephen M Trimberger, "Field Programmable Gate Array Technology", Springer international Edition, 2007.
3. Stephen D Brown, R.Francis, J.Rose, Z.Vranesic, "Field Programmable Gate Array", Springer, 1992.

REFERENCES:

1. J. Old Field, R.Dorf, "Field Programmable Gate Arrays", John Wiley &Sons,2008.
2. Ian Grout, "Digital Systems Design with FPGAs and CPLDs", Elsevier, Newnes,2008.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	2	2	2	2	3	3	
CO2	3	3	3	3	3	3	3	
CO3	3	2	3	2	2	2	3	
CO4	3	2	3	3	3	3	3	3

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L	T	P	C
3	0	0	3

(20BVL24) TESTING & TESTABILITY
(ELECTIVE-V)

Outcomes:

On successful completion of the course the student will be able to:

1. Describe the levels of modeling in digital circuits.
2. Get knowledge on single stuck faults and multiple stuck faults.
3. Understand the different testing architectures.
4. Identify faulty components with in a circuit.

UNIT I

INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT) FUNDAMENTALS: Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models, Levels of Modeling, Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

UNIT II

FAULT MODELING: Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location, Single Stuck and Multiple Stuck – Fault Models, Fault Simulation Applications, General Techniques for Combinational Circuits.

TESTING FOR SINGLE STUCK FAULTS (SSF): Automated Test Pattern Generation (ATPG/ATG) For SSFs in Combinational and Sequential Circuits, Functional Testing With Specific Fault Models

UNIT III

DESIGN FOR TESTABILITY: Testability Trade-Offs, Techniques, Scan Architectures and Testing – Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design, Board Level and System Level DFT Approaches, Boundary Scans Standards, Compression Techniques – Different Techniques, Syndrome Test and Signature Analysis.

UNIT IV

BUILT-IN SELF-TEST (BIST): BIST Concepts and Test Pattern Generation, Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO, Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level.

UNIT V

MEMORY BIST (MBIST): Memory Test Architectures and Techniques – Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model, Memory Test Requirements for MBIST.

BRIEF IDEAS ON EMBEDDED CORE TESTING: Introduction to Automatic in Circuit Testing (ICT), JTAG Testing Features.

TEXT BOOKS:

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, "Digital Systems Testing and Testable Design", Jaico Publishing House, 2001.
2. Alfred Crouch, "Design for Test for Digital ICs & Embedded Core Systems", PrenticeHall.

REFERENCES:

1. Robert J.Feugate, Jr., Steven M.Mentyn, "Introduction to VLSI Testing", Prentice Hall, Englehood Cliffs, 1998.
2. M.L. Bushnell, V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits", Kluwer Academic Pulishers.
3. P.K. Lala, "Digital Circuits Testing and Testability", AcademicPress.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	3	3	3	2	3	3	
CO2	3	3	3	3	2	3	3	
CO3	3	3	3	3	3	3	3	
CO4	3	3	3	3	2	3	3	

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M.Tech- III Semester-VLSI Design

L	T	P	C
3	0	0	3

(20BVL25) ASIC DESIGN
(ELECTIVE-V)

Outcomes:

On successful completion of the course the student will be able to

1. Gain knowledge on the basics of ASIC design styles and FPGA.
2. Understand Design flow and methodologies.
3. Familiar with the various design aspects, logic synthesis, simulation and testing.
4. Understand XILINX, ALTERA tools.

UNIT I

ASICs - DESIGN STYLES: Introduction, Categories, Gate Arrays, Standard Cells, Cell Based ASICs, Mixed Mode and Analogue ASICs, PLDs.

ASICs – PROGRAMMABLE LOGIC DEVICES: Overview, PAL based PLDS Structures, PAL Characteristics, FPGAS: Introduction, Selected Families, Design Outline.

UNIT II

ASICs – DESIGN ISSUES: Design Methodologies and Design Tools, Design for Testability, Economies.

ASICs - CHARACTERISTICS AND PERFORMANCE: Design Styles, Gate Arrays, Standard Cell based ASICS, Mixed Mode and Analogue ASICs.

UNIT III

ASICs-DESIGN TECHNIQUES: Overview- Design Flow and Methodology, Hardware Description Languages, Simulation and Checking, Commercial Design Tools, FPGA Design Tools: XILINX, ALTERA

UNIT IV

LOGIC SYNTHESIS, SIMULATION AND TESTING: Verilog and Logic Synthesis -VHDL and Logic Synthesis, Types of Simulation, Boundary Scan Test, Fault Simulation, Automatic Test Pattern Generation.

UNIT V

ASIC CONSTRUCTION: Floor Planning, Placement and Routing, System Partition.

FPGA PARTITIONING: Partitioning Methods, Floor Planning, Placement, Physical Design Flow, Global Routing, Detailed Routing, Special Routing, Circuit Extraction, DRC.

TEXT BOOKS:

1. L.J. Herbst, "Integrated Circuit Engineering", OXFORD SCIENCE Publications, 1996.
2. K. Eshraghian et . al, "Essentials of VLSI Circuits and Systems", PHI of India Ltd.,2005
3. Wayne Wolf, "Modern VLSI Design", Pearson Education, Fifth Indian Reprint, 3rd Edition, 2005.

References:

1. M.J.S.Smith, "Application - Specific Integrated Circuits", Addison-Wesley Longman Inc 1997.
2. Douglas A Pucknell, Weste, K.Eshraghian, "Basic VLSI Design", PHI, 3rd Edition.
3. Fabricius, "Introduction to VLSI Design", MGH International Edition, 1990.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	1	1	3	2	1	2	3	
CO2	2	2	3	2	2	3	3	
CO3	3	2	3	3	2	3	3	
CO4	2	1	1	1	1	3	3	

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M.Tech-III Semester- VLSI Design

(20BVL26) HIGH SPEED NETWORKS

(ELECTIVE – VI)

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3	0	0	3

Outcomes:

On successful completion of the course the student will be able to

1. Design the different technologies involved in High Speed Networking and their performance.
2. Understand switching in ATM and Frame Relay networks.
3. Develop an in-depth understanding, in terms of architecture, protocols and applications of major high-speed networking technologies.
4. Solve numerical or analytical problems pertaining to the high-speed networking technologies.

UNIT I

NETWORK SERVICES & LAYERED ARCHITECTURE: Traffic Characterization and Quality of Service, Network Services, High Performance Networks, Network Elements, Basic Network Mechanisms, Layered Architecture, QoS in IP Networks, Differentiated and Integrated Services.

UNIT II

ISDN & B-ISDN: Over view of ISDN, ISDN channels, User access, ISDN Protocols, Brief history of B-ISDN and ATM, ATM based Services and Applications, Principles and building block of B-ISDN, General Architecture of B-ISDN, Frame Relay.

UNIT III

ATM NETWORKS: Network Layering, Switching of Virtual Channels and Virtual Paths, Applications of Virtual Channels and Connections, QoS Parameters, Traffic Descriptors, ATM Service Categories, ATM Cell Header, ATM Layer, ATM Adaptation Layer.

UNIT IV

INTERCONNECTION NETWORKS: Introduction, Banyan Networks, Routing algorithm & Blocking Phenomenon, Batcher-Banyan Networks, Crossbar Switch, Three Stage Class Networks.

RE-ARRANGEABLE NETWORKS: Rearrangeable Class Networks, Folding Algorithm, Bens Network, Looping Algorithm.

UNIT-V

ATM SIGNALING, ROUTING AND TRAFFIC CONTROL: ATM addressing, UNI signaling, PNNI signaling, PNNI routing, ABR Traffic management.

TCP/IP NETWORKS: History of TCP/IP, TCP Application and Services, Motivation, TCP, UDP, IP Services and Header Formats, Internetworking, TCP Congestion Control, Queue Management: Passive & Active.

TEXT BOOKS:

1. William Stallings, "ISDN & B-ISDN with Frame Relay", PHI.
2. Leon Garcia widjaja, "Communication Networks", TMH, 2000.
3. 3. N. N. Biswas, "ATM Fundamentals", Adventure books publishers.

REFERENCES:

1. Warland & Pravin Varaiya, "High Performance Communication Networks", Jean Hardout Asia Pvt. Ltd.,II Edition,2001.
2. William Stallings, "High Speed Networks And Internet", Pearson Education, Second Edition, 2002.
3. Abhijit S. Pandya, Ercan Sea"ATM Technology for Broad Band Telecommunication Networks", CRC Press, New York, 2004

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	2	3	1	3	1	2	3	
CO2	2	3	2	3	1	2	3	
CO3	2	3	3	3	1	2	3	
CO4	2	3	3	3	1	2	3	

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M.Tech- III Semester- VLSI Design

L	T	P	C
3	0	0	3

(20BVL27) SYSTEM ON CHIP DESIGN AND VERIFICATION

Outcomes:

On successful completion of the course the student will be able to

1. Gain knowledge about SOC design and architecture.
2. Understand about the design process and issues.
3. Understand about embedded memories.
4. Analyze about various on chip protocols and implementation.

UNIT I

INTRODUCTION TO THE SOC APPROACH: System Architecture, Processor Architectures, Memory and Addressing, Review of Moore's law and CMOS Scaling, Comparison on System-on-Board, System-on-Chip, and System-in-Package- benefits of system-on-chip integration in terms of cost, power, and performance - SOC Design, Platform-Based SoC Design., Multiprocessor SoC and Network on Chip, Low-Power SoC Design, System Architecture and Complexity SoC Design.

UNIT II

PROCESSORS & SYSTEM ON CHIP DESIGN PROCESS: Processor Selection for SOC, Robust Processors- Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors- A canonical SoC Design, SoC Design flow waterfall vs spiral, top down vs Bottom up- Specification requirement, Types of Specification , System Design process and design issues, Soft IP Vs Hard IP, IP verification and integration, hardware-software co-design, Design for timing closure, Logic design issues Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in an SOC.

UNIT III

EMBEDDED MEMORIES: Overview of SOC external memory, Internal Memory, Scratchpads and Cache memory, Cache Organizat ion, Cache data, Write Policies, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, memory interaction, Cache coherence, MESI protocol and Directory-based coherence.

UNIT IV

NOC-BASED SOC: Network on Chip (NOC), Architecture of NoC -Network on Chip topologies-Mesh-based NoC.-Routing in an NoC- Packet switching and wormhole routing-NoC Protocol Design, Low-Power Design for NoC, Low-Power Network on Chip Protocol, Low-Power channel Coding,Low-Power Clocking, Low-Power Signaling, On-Chip Serialization.

UNIT V

NOC / MPSOCS: Real Chip Implementation-BONE Series, Industrial Implementations-,Intel's Tera-FLOP 80-Core NoC, MPSoCs. Techniques for designing MPSoCs, Performance

and flexibility for MPSoCs design.
Case study: A Low Power Open Multimedia Application Platform for 3G Wireless

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley
3. Hoi-jun yoo, Kangmin Lee, Jun Kyoung kim, "Low power NoC for high performance SoC desing",CRC press, 2008.

REFERENCES:

1. Vijay K. Madisetti Chonlameth Arpikanondt, "A Platform-Centric Approach to System-on-Chip (SOC) Design", Springer, 2005.
2. Sudeep Pasricha and Nikil Dutt,"On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers © 2008
3. Ahmed Amine Jeraya, Wayne Wolf, "Multiprocessor System On chip", Morgan Kauffmann, 2005.
4. James K. Peckol, "Embedded Systems: A Contemporary Design Tool", WILEY Student Edition.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PS02
CO1	3	3	3	3	2	2	3	
CO2	3	3	3	3	2	3	3	
CO3	3	3	3	1	2	2	3	
CO4	3	3	3	3	2	2	3	

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M.Tech- III Semester- VLSI Design	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(20BVL28) RF IC DESIGN

Course Outcomes:

On successful completion of the course the student will be able to

1. Demonstrate in-depth knowledge in Radio Frequency Integrated Circuits.
2. Analyze complex engineering problems critically for conducting research in RF systems.
3. Solve engineering problems with wide range of solutions in Radio Frequency Integrated circuits.
4. Apply appropriate techniques to engineering activities in the field of RFIC Design.

UNIT-I BASIC CONCEPTS IN RF DESIGN

Introduction to RF Design, Units in RF design, Time Variance and Nonlinearity, Effects of nonlinearity, random processes and Noise, Definitions of sensitivity and dynamic range, Passive impedance transformation, Scattering parameters.

UNIT-II TRANSCEIVER ARCHITECTURES

General considerations, Receiver Architectures-Basic Heterodyne receivers, Modern heterodyne receivers, Direct conversion receivers, Image-Reject receivers, Low-IF receivers. Transmitter Architectures-Direct Conversion transmitters, Modern direct conversion Transmitters, Heterodyne Transmitters, Other Transmitter Architectures.

UNIT-III LNA AND MIXERS

General considerations, Problem of input matching, Low Noise Amplifiers design in various topologies, Gain Switching, Band Switching, Mixers-General considerations, Passive down conversion mixers, Active down conversion mixers, Up conversion mixers.

UNIT- IV OSCILLATORS

Performance parameters, Basic principles, Cross coupled oscillator, Three point oscillators, Voltage Controlled Oscillators, LC VCOs with wide tuning range, phase noise, Mathematical model of VCOS, Quadrature Oscillators.

UNIT V PLL AND POWER AMPLIFIER

PLLS-Phase detector, Type-I PLLs, Type-II PLLs, PFD/CP Nonidealities, Phase noise in PLLs, Loop Bandwidth. Power Amplifiers-General considerations, Classification of power amplifiers, High-Efficiency power amplifiers, Cascode output stages, Large signal impedance matching, Linearization techniques.

Text Books:

1. B.Razavi, “RF Microelectronics”, Prentice-Hall PTR, 2nd Edition, 1998.

Reference Books:

1. T.H.Lee, “The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2nd, 1998
2. R.Jacob Baker, Harry W.Li, D.E. Boyce, “CMOS Circuit Design, Layout and Simulation”, Prentice-Hall of India, 1998.

	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	3	3	3	3	3	3	3	3
CO2	3	3	2	3	3	3	3	3	3
CO3	3	3	2	3	3	3	3	3	3
CO4	3	3	3	3	3	3	3	3	3

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3	0	0	3

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L	T	P	C
0	0	20	10

M.Tech- III Semesters - VLSI Design

(20BVL29) DISSERTATION PHASE-I

Sri Venkateswara College of Engineering and Technology, Chittoor.
(Autonomous)

M.Tech- IV Semesters - VLSI Design

L	T	P	C
0	0	32	16

(20BVL30) DISSERTATION PHASE-II